

## 5-V, WPC1.1 Compliant Wireless Power Transmitter Manager

 Check for Samples: [bq500211A](#)

### FEATURES

- **Intelligent Control of Wireless Power Transfer**
- **5-V Operation Conforms to Wireless Power Consortium (WPC) Type A5 and Type A11 Transmitter Specifications**
- **WPC1.1 Compliant, Including Foreign Object Detection (FOD)**
- **Enhanced Parasitic Metal Detection (PMOD) Assures Safety**
- **Dynamic Power Limiting™ for USB and Limited Source Operation**
- **Digital Demodulation Reduces Components**
- **LED Indication of Charging State and Fault Status**

### APPLICATIONS

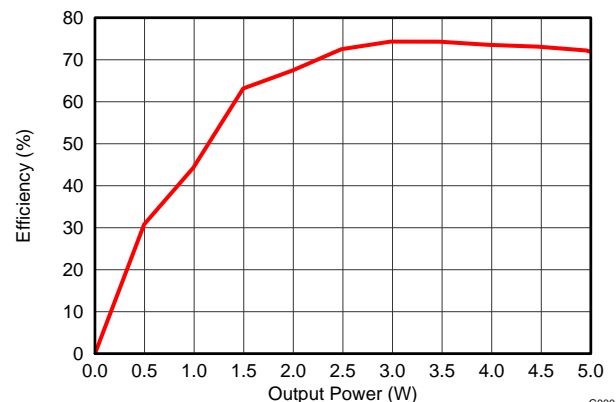
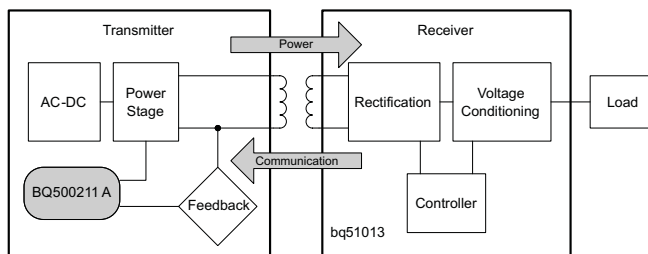
- **WPC 1.1 Compliant Wireless Chargers For:**
  - **Qi-Certified Smart Phones and other Handhelds**
  - **Hermetically Sealed Devices and Tools**
  - **Cars and Other Vehicles**
  - **Tabletop Charge Surfaces**
- See [www.ti.com/wirelesspower](http://www.ti.com/wirelesspower) for More Information on TI's Wireless Charging Solutions

### DESCRIPTION

The bq500211A is a second generation digital wireless power controller that integrates all functions required to control wireless power transfer to a single WPC compliant receiver. It is WPC1.1 compliant and designed for 5-V systems as either a WPC type A5 transmitter with a magnetic positioning guide or as a WPC type A11 transmitter without the magnetic guide. The bq500211A *pings* the surrounding environment for WPC compliant devices to be powered, safely engages the device, receives packet communication from the powered device and manages the power transfer. To maximize flexibility in wireless power applications, Dynamic Power Limiting™ (DPL) is featured on the bq500211A. DPL enhances user experience by seamlessly optimizing the usage of power available from limited input supplies. The bq500211A supports both Foreign Object Detection (FOD) and Parasitic Metal Object Detection (PMOD) by continuously monitoring the efficiency of the established power transfer, protecting from power lost due to metal objects misplaced in the wireless power transfer bath. Should any abnormal condition develop during power transfer, the bq500211A handles it and provides indicator outputs. Comprehensive status and fault monitoring features enable a robust system design.

The bq500211A is available in a 48-pin, 7 mm x 7 mm QFN package and operates over a temperature range from  $-40^{\circ}\text{C}$  to  $110^{\circ}\text{C}$ .

### Functional Diagram and Efficiency Versus System Output Power



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Dynamic Power Limiting is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup>

OPERATING TEMPERATURE RANGE, T <sub>A</sub>	ORDERABLE PART NUMBER	PIN COUNT	SUPPLY	PACKAGE	TOP SIDE MARKING
-40°C to 110°C	bq500211ARGZR	48 pin	Reel of 2500	QFN	bq500211A
	bq500211ARGZT	48 pin	Reel of 250	QFN	bq500211A

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	VALUE		UNIT
	MIN	MAX	
Voltage applied at V33D to GND	-0.3	3.6	V
Voltage applied at V33A to GND	-0.3	3.6	
Voltage applied to any pin <sup>(2)</sup>	-0.3	3.6	
Storage temperature, T <sub>STG</sub>	-40	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to GND.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V	Supply voltage during operation, V33D, V33A	3.0	3.3	3.6	V
T <sub>A</sub>	Operating free-air temperature range	-40		110	°C
T <sub>J</sub>	Junction temperature			110	

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	bq500211A		UNITS
	RGZ		
	48 PINS		
θ <sub>JA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	28.4	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance <sup>(3)</sup>	14.2	
θ <sub>JB</sub>	Junction-to-board thermal resistance <sup>(4)</sup>	5.4	
ψ <sub>JT</sub>	Junction-to-top characterization parameter <sup>(5)</sup>	0.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter <sup>(6)</sup>	5.3	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	1.4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

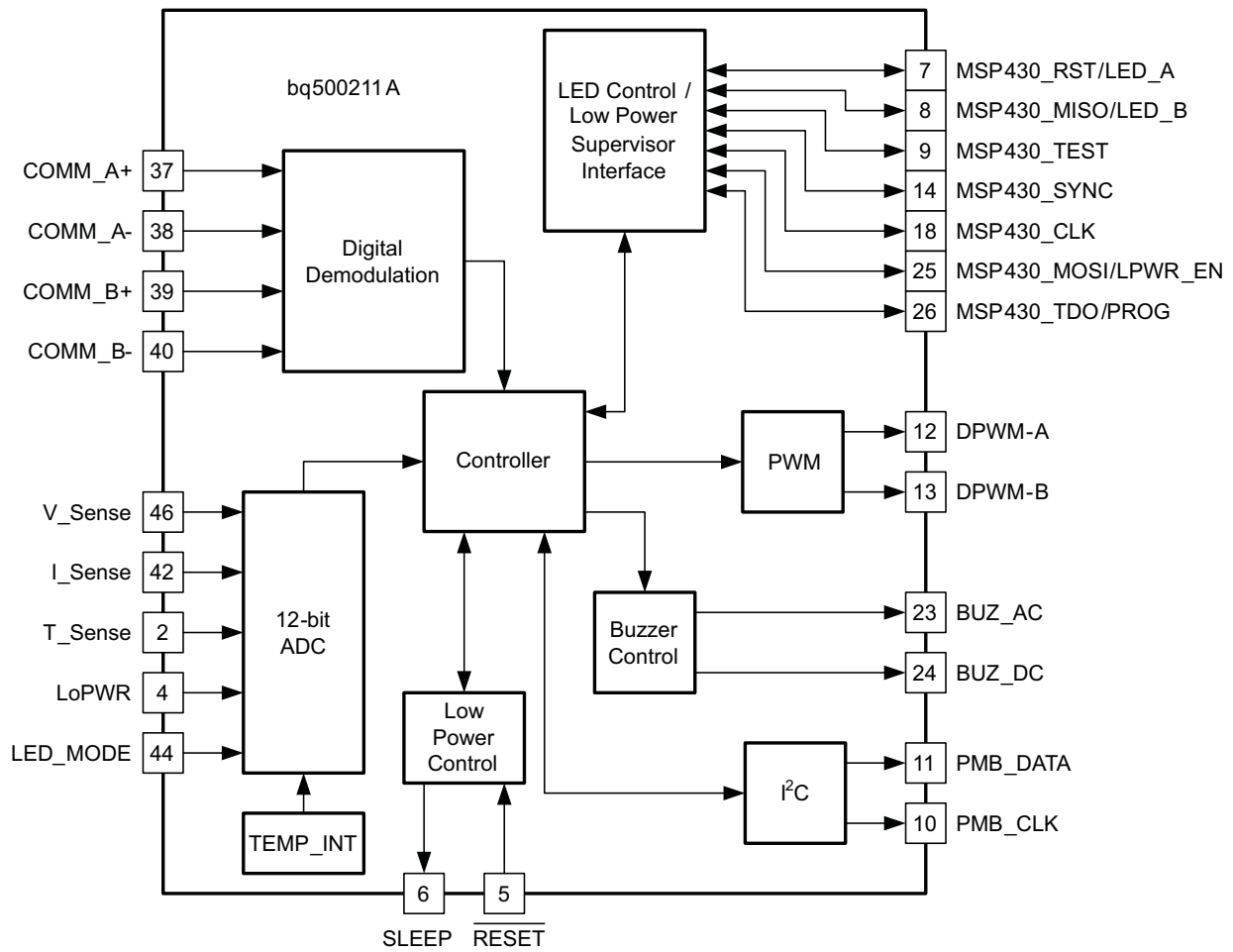
## ELECTRICAL CHARACTERISTICS

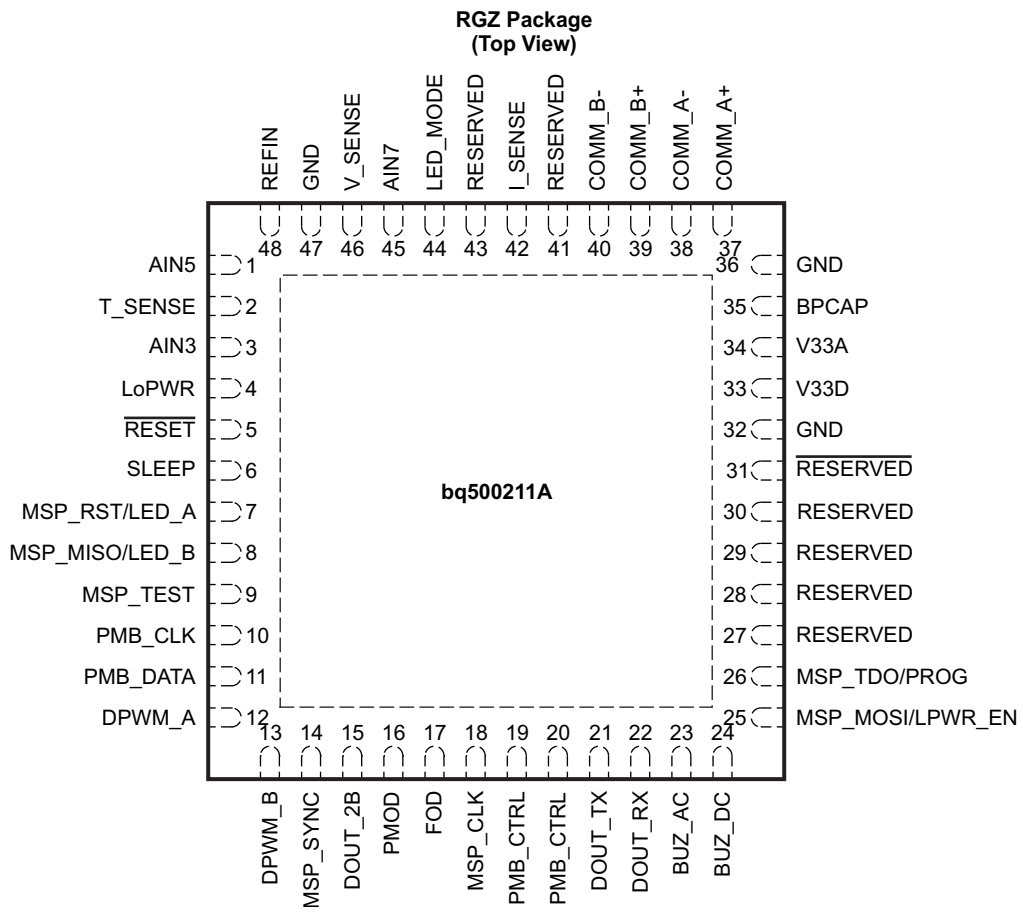
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{V33A}$	Supply current	V33A = 3.3 V		8	15	mA
$I_{V33D}$		V33D = 3.3 V		44	55	
$I_{TOTAL}$		V33D = V33A = 3.3 V		52	60	
<b>INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS</b>						
V33	3.3-V linear regulator	Emitter of NPN transistor	3.25	3.3	3.6	V
V33FB	3.3-V linear regulator feedback			4	4.6	
$I_{V33FB}$	Series pass base drive	$V_{IN} = 12$ V; current into V33FB pin		10		mA
Beta	Series NPN pass device		40			
<b>EXTERNALLY SUPPLIED 3.3 V POWER</b>						
V33D	Digital 3.3-V power	$T_A = 25^\circ\text{C}$	3		3.6	V
V33A	Analog 3.3-V power	$T_A = 25^\circ\text{C}$	3		3.6	
V33Slew	V33 slew rate	V33 slew rate between 2.3 V and 2.9 V, V33A = V33D	0.25			V/ms
<b>DIGITAL DEMODULATION INPUTS COMM_A+, COMM_A-, COMM_B+, COMM_B-</b>						
$V_{CM}$	Common mode voltage each pin		-0.15		1.631	V
COMM+, COMM-	Modulation voltage digital resolution			1		mV
$R_{EA}$	Input impedance	Ground reference	0.5	1.5	3	M $\Omega$
$I_{OFFSET}$	Input offset current	1-k $\Omega$ source impedance	-5		5	$\mu\text{A}$
<b>ANALOG INPUTS V_SENSE, I_SENSE, T_SENSE, LED_MODE</b>						
$V_{ADDR\_OPEN}$	Voltage indicating open pin	LED_MODE open	2.37			V
$V_{ADDR\_SHORT}$	Voltage indicating pin shorted to GND	LED_MODE shorted to ground			0.36	
$V_{ADC\_RANGE}$	Measurement range for voltage monitoring	ALL ANALOG INPUTS	0		2.5	
INL	ADC integral nonlinearity		-2.5		2.5	mV
$I_{lkg}$	Input leakage current	3 V applied to pin			100	nA
$R_{IN}$	Input impedance	Ground reference	8			M $\Omega$
$C_{IN}$	Input capacitance				10	pF
<b>DIGITAL INPUTS/OUTPUTS</b>						
$V_{OL}$	Low-level output voltage	$I_{OL} = 6$ mA, V33D = 3 V			DGND1 + 0.25	V
$V_{OH}$	High-level output voltage	$I_{OH} = -6$ mA, V33D = 3 V		V33D - 0.6V		
$V_{IH}$	High-level input voltage	V33D = 3V	2.1		3.6	
$V_{IL}$	Low-level input voltage	V33D = 3.5 V			1.4	
$I_{OH}(MAX)$	Output high source current				4	mA
$I_{OL}(MAX)$	Output low sink current				4	
<b>SYSTEM PERFORMANCE</b>						
$V_{RESET}$	Voltage where device comes out of reset	V33D Pin	2.3		2.4	V
$t_{RESET}$	Pulse width needed for reset	RESET pin	2			$\mu\text{s}$
$f_{SW}$	Switching Frequency		112		205	kHz
$t_{detect}$	Time to detect presence of device requesting power				0.5	s
$t_{retention}$	Retention of configuration parameters	$T_J = 25^\circ\text{C}$	100			Years

DEVICE INFORMATION

Functional Block Diagram





**PIN FUNCTIONS**

PIN		I/O	DESCRIPTION
NO.	NAME		
3	AIN3	I	This pin can be either connected to GND or left open. Connecting to GND can improve layout grounding.
1	AIN5	I	This pin can be either connected to GND or left open. Connecting to GND can improve layout grounding.
45	AIN7	I	This pin can be either connected to GND or left open. Connecting to GND can improve layout grounding.
35	BPCAP	—	Bypass capacitor for internal 1.8-V core regulator. Connect bypass capacitor to GND.
23	BUZ_AC	O	AC Buzzer Output. Outputs a 400-ms, 4-kHz AC pulse when charging begins.
24	BUZ_DC	O	DC Buzzer Output. Outputs a 400-ms DC pulse when charging begins. This could also be connected to an LED via 470-Ω resistor.
37	COMM_A+	I	Digital demodulation non-inverting input A, connect parallel to input B+.
38	COMM_A-	I	Digital demodulation inverting input A, connect parallel to input B-.
39	COMM_B+	I	Digital demodulation non-inverting input B, connect parallel to input A+.
40	COMM_B-	I	Digital demodulation inverting input B, connect parallel to input A-.
22	DOUT_RX	I	Leave this pin open.
21	DOUT_TX	I	Leave this pin open.
15	DOUT_2B	O	Optional Logic Output 2B. Leave this pin open.
12	DPWM_A	O	PWM Output A, controls one half of the full bridge in a phase-shifted full bridge. Switching deadtimes must be externally generated.
13	DPWM_B	O	PWM Output B, controls other half of the full bridge in a phase-shifted full bridge. Switching deadtimes must be externally generated.
49	EPAD	-	Flood with copper GND plane and stitch vias to PCB internal GND plane.
17	FOD	O	FOD read pin. Leave open unless PMOD and FOD thresholds need to be different. It controls the FOD threshold resistor read at startup.
32	GND	—	GND.
36	GND	—	GND.
47	GND	—	GND.
42	I_SENSE	I	Transmitter input current, used for efficiency calculations. Use 20-mΩ sense resistor and A=50 gain current sense amplifier.
44	LED_MODE	I	Input to select from 4 LED modes.
4	LoPWR	I	Dynamic Power Limiting™ (DPL) control pin. To set power mode to 500 mA, pull to GND. For full-power operation pull to 3.3-V supply.
43	LOSS_THR	I	Input to program foreign and parasitic metal object detection threshold
18	MSP_CLK	I/O	Used for boot loading the MSP430 low power supervisor. If MSP430 is not used, leave this pin floating.
8	MSP_MISO/LED_B	I	MSP – TMS, SPI-MISO, LED-B -- If external MSP430 is not used, connect to an LED via 470-Ω resistor for status indication.
7	MSP_RST/LED_A	I	MSP – Reset, LED-A -- If external MSP430 is not used, connect to an LED via 470-Ω resistor for status indication.
14	MSP_SYNC	O	MSP SPI_SYNC, if external MSP430 is not used, leave this pin open.
26	MSP_TDO/PROG	I/O	MSP-TDO, MSP430 programmed indication.
9	MSP_TEST	I	MSP – Test, If external MSP430 is not used, leave this pin open.
25	MSP_MOSI/LPWR_EN	I/O	Low standby power supervisor enable. If low power is not needed, connect this to GND.
16	PMOD	O	PMOD read pin. Leave open unless PMOD and FOD thresholds need to be different. It controls the PMOD threshold resistor read at startup.
10	PMB_CLK	I/O	10-kΩ pull-up resistor to 3.3-V supply.
11	PMB_DATA	I/O	10-kΩ pull-up resistor to 3.3-V supply.

**PIN FUNCTIONS (continued)**

PIN		I/O	DESCRIPTION
NO.	NAME		
19	RESERVED	O	Reserved, leave this pin open.
20	RESERVED	I	Reserved, connect to GND.
48	RESERVED	I	External Reference Voltage Input. Connect this input to GND.
27	RESERVED	I/O	Reserved, leave this pin open.
28	RESERVED	I/O	Reserved, leave this pin open.
29	RESERVED	I/O	Reserved, leave this pin open.
30	RESERVED	I/O	Reserved, leave this pin open.
31	RESERVED	I/O	Reserved, connect 10-kΩ pull-down resistor to GND.
41	RESERVED	O	Reserved, leave this pin open.
5	RESET	I	Device reset. Use a 10-kΩ to 100-kΩ pull-up resistor to the 3.3-V supply.
6	SLEEP	O	Low-power mode output. Starts low-power ping cycle.
2	T_SENSE	I	Sensor Input. Device shuts down when below 1 V. If not used, keep above 1 V by connecting to the 3.3-V supply.
46	V_SENSE	I	Transmitter input voltage, used for efficiency calculations. Use 76.8-kΩ to 10-kΩ divider to minimize quiescent current.
34	V33A	—	Analog 3.3-V Supply. This pin can be derived from V33D supply, decouple with 10-Ω resistor and additional bypass capacitors
33	V33D	—	Digital core 3.3-V supply. Be sure to decouple with bypass capacitors as close to the part as possible.

**Typical Characteristics Curves**

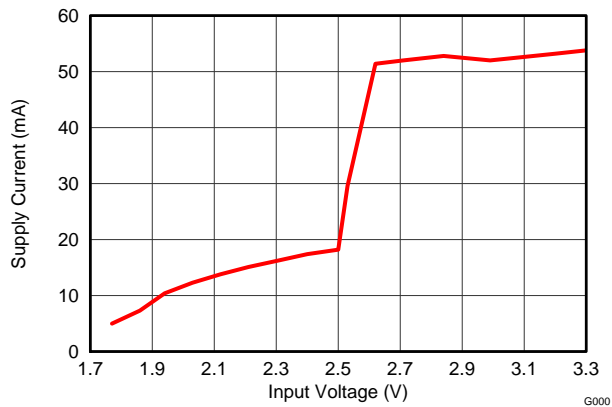


Figure 1. bq500211A Supply Current vs. VCC Voltage

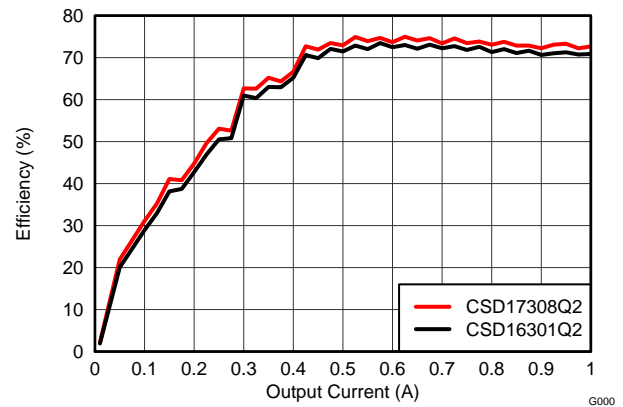


Figure 2. System Efficiency Using Alternate MOSFETs



## Principles of Operation

### Fundamentals

The principle of wireless power transfer is simply an open cored transformer consisting of primary and secondary coils and associated electronics. The primary coil and electronics are also referred to as the transmitter, and the secondary side the receiver. The transmitter coil and electronics are typically built into a charger pad. The receiver coil and electronics are typically built into a portable device, such as a cell-phone.

When the receiver coil is positioned on the transmitter coil, magnetic coupling occurs when the transmitter coil is driven. The flux is coupled into the secondary coil which induces a voltage, current flows, it is rectified and power can be transferred quite effectively to a load - wirelessly. Power transfer can be managed via any of various familiar closed-loop control schemes.

### Wireless Power Consortium (WPC)

The Wireless Power Consortium (WPC) is an international group of companies from diverse industries. The WPC standard was developed to facilitate cross compatibility of compliant transmitters and receivers. The standard defines the physical parameters and the communication protocol to be used in wireless power. For more information, go to [www.wirelesspowerconsortium.com](http://www.wirelesspowerconsortium.com).

### Power Transfer

Power transfer depends on coil coupling. Coupling is dependant on the distance between coils, alignment, coil dimensions, coil materials, number of turns, magnetic shielding, impedance matching, frequency and duty cycle.

Most importantly, the receiver and transmitter coils must be aligned for best coupling and efficient power transfer. The closer the space between the coils, the better the coupling, but the practical distance is set to be less than 5 mm (as defined within the WPC Specification) to account for housing and interface surfaces.

Shielding is added as a backing to both the transmitter and receiver coils to direct the magnetic field to the coupled zone. Magnetic fields outside the coupled zone do not transfer power. Thus, shielding also serves to contain the fields to avoid coupling to other adjacent system components.

Regulation can be achieved by controlling any one of the coil coupling parameters. For WPC compatibility, the transmitter coils and capacitance are specified and the resonant frequency point is fixed at 100 kHz. Power transfer is regulated by changing the operating frequency between 112 kHz to 205 kHz. The higher the frequency, the further from resonance and the lower the power. Duty cycle remains constant at 50% throughout the power band and is reduced only once 205 kHz is reached.

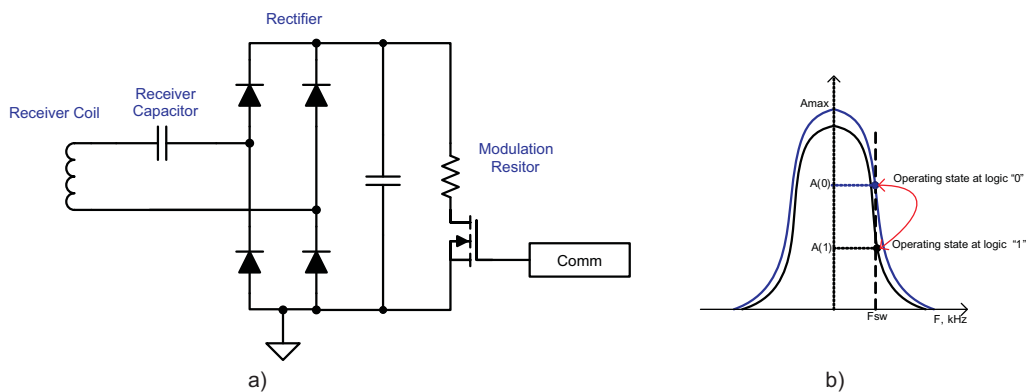
The WPC standard describes the dimension and materials of the coils. It also has information on tuning the coils to resonance. The value of the inductor and resonant capacitor are critical to proper operation and system efficiency.

### Communication

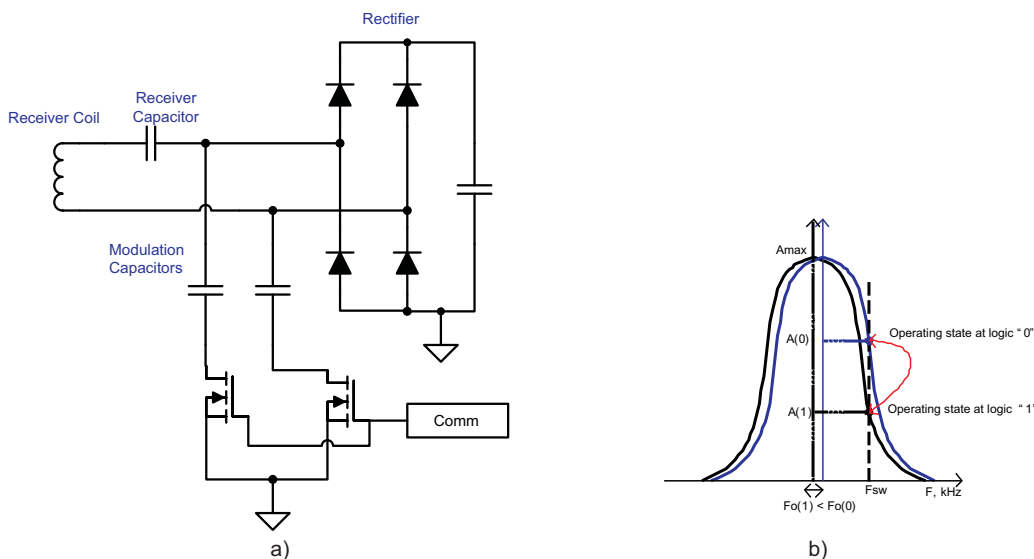
Communication within the WPC is from the receiver to the transmitter, where the receiver tells the transmitter to send power and how much. In order to regulate, the receiver must communicate with the transmitter whether to increase or decrease frequency. The receiver monitors the rectifier output and using Amplitude Modulation (AM), sends packets of information to the transmitter. A packet is comprised of a preamble, a header, the actual message and a checksum, as defined by the WPC standard.

The receiver sends a packet by modulating an impedance network. This AM signal reflects back as a change in the voltage amplitude on the transmitter coil. The signal is demodulated and decoded by the transmitter side electronics and the frequency of its coil drive output is adjusted to close the regulation loop. The bq500211A features internal digital demodulation circuitry.

The modulated impedance network on the receiver can either be resistive or capacitive. **Figure 3** shows the resistive modulation approach, where a resistor is periodically added to the load and also shows the resulting change in resonant curve which causes the amplitude change in the transmitter voltage indicated by the two operating points at the same frequency. **Figure 4** shows the capacitive modulation approach, where a capacitor is periodically added to the load and also shows the resulting amplitude change in the transmitter voltage.



**Figure 3. Receiver Resistive Modulation Circuit**



**Figure 4. Receiver Capacitive Modulation Circuit**

## Application Information

### Coils and Matching Capacitors

The coil and matching capacitor selection for the transmitter has been established by WPC standard. This is fixed and cannot be changed on the transmitter side.

An up to date list of available and compatible A5 and A11 transmitter coils can be found here ([Texas Instruments Literature Number SLUA649](#)):

Capacitor selection is critical to proper system operation. A total capacitance value of 400 nF is required in the resonant tank. This is the WPC system compatibility requirement, not a guideline, and must be followed.

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#### NOTE

A total capacitance value of 400 nF/50 V (C0G dielectric type or equivalent) is required in the resonant tank to achieve a 100-kHz resonance frequency.

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The capacitors chosen must be rated for at least 50 V and must be of high quality C0G dielectric or equivalent. These are typically available in a 5% tolerance. The use of X7R types or below is not recommended if WPC compliance is required because critical WPC certification testing, such as the minimum modulation requirement, might fail.

A 400-nF capacitor is not a standard value and therefore several must be combined in parallel. The designer can combine a (4 nF x 100 nF) or a (180 nF + 220 nF) along with other combinations depending on market availability. All capacitors must be of high quality C0G type or equivalent and not mixed with lesser dielectric types.

### Dynamic Power Limiting™

Dynamic Power Limiting™ (DPL) allows operation from a 5-V supply with limited current capability (such as a USB port). There are two modes of operation selected via an input pin. In the dynamic mode, when the input voltage is observed drooping, the output power is limited to reduce the load and provides margin relative to the supply's capability. The second mode, or constant current mode, is designed specifically for operation from a 500-mA capable USB port, it restricts the output such that the input current remains below the 500-mA limit.

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#### NOTE

Pin 4 must always be terminated, else erratic behavior may result.

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Anytime the DPL control loop is regulating the operating point of the transmitter, the LED will indicate that DPL is active. The LED color and flashing pattern are determined by the LED Table. If the receiver sends a Control Error Packet (CEP) with a negative value, (for example, to reduce power to the load), the WPTX in DPL mode will respond to this CEP via the normal WPC control loop.

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#### NOTE

Depending on LED\_MODE selected, the power limit indication may be either solid amber (green + red) or solid red.

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### Option Select Pin

Two pins (pin 43 and pin 44) on the bq500211A are allocated to program the Loss Threshold and the LED mode of the device. At power up, a bias current is applied to pins LED\_MODE and LOSS\_THR and the resulting voltage measured in order to identify the value of the attached programming resistor. The values of the operating parameters set by these pins are determined using Table 2. For LED\_MODE, the selected bin determines the LED behavior based on Table 1; for the LOSS\_THR, the selected bin sets a threshold used for parasitic metal object detection (see Parasitic Metal Detection (PMOD) and Foreign Object Detection (FOD) section). Table 1.

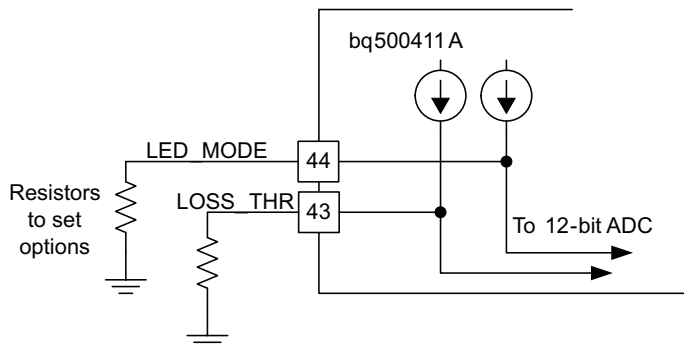


Figure 5. Option Select Pin Programming

### LED Indication Modes

The bq500211A can directly drive two LED outputs (pin 7 and pin 8) through a simple current limit resistor (typically 470 Ω), based on the mode selected. The two current limit resistors can be individually adjusted to tune or match the brightness of the two LEDs. Do not exceed the maximum output current rating of the device.

The resistor in Figure 5 connected to pin 44 and GND selects the desired LED indication scheme in Table 1.

Table 1. LED Modes

LED CONTROL OPTION	LED SELECTION RESISTOR	DESCRIPTION	LED	Operational States				
				STANDBY	POWER TRANSFER	CHARGE COMPLETE	FAULT	DYNAMIC POWER LIMITING™
X	< 36.5 kΩ	Reserved, do not use	LED1, green	-	-	-	-	-
			LED2, red	-	-	-	-	-
1	42.2 kΩ	Choice number 1	LED1, green	Off	Blink slow	On	Off	Blink slow
			LED2, red	Off	Off	Off	On	Blink slow
2	48.7 kΩ	Choice number 2	LED1, green	On	Blink slow	On	Off	Blink slow
			LED2, red	On	Off	Off	On	Blink slow
3	56.2 kΩ	Choice number 3	LED1, green	Off	Off	On	Off	Off
			LED2, red	Off	On	Off	Blink slow	On
4	64.9 kΩ	Choice number 4	LED1, green	Off	On	Off	Off	Off
			LED2, red	Off	Off	Off	On	Blink slow
	> 75 kΩ	Reserved, all LED off	-	-	-	-	-	

## Parasitic Metal Object Detect (PMOD) and Foreign Object Detection (FOD)

The bq500211A is WPC1.1 compliant and supports both enhanced PMOD and the new FOD features by continuously monitoring the input voltage and current to calculate input power. Combining input power, known losses, and the value of power reported by the RX device being charged, the bq500211A can estimate how much power is unaccounted for and presumed lost due to metal objects placed in the wireless power transfer path. If this unexpected loss exceeds the threshold set by the LOSS\_THR resistor, a fault is indicated and power transfer is halted. Whether the PMOD or the FOD algorithm is used is determined by the ID packet of the receiver being charged.

PMOD has certain inherent weaknesses as rectified power is not ensured to be accurate per WPC1.0 Specification. The user has the flexibility to adjust the LOSS\_THR resistor to suit the application. Should issues with compliance or interoperability arise, the PMOD feature can be selectively disabled as explained below.

The FOD algorithm uses information from an in-system characterized and WPC1.1 certified RX and it is therefore more accurate. Where the WPC1.0 specification merely requires the Rectified Power packet, the WPC1.1 specification additionally uses the Received Power packet which more accurately tracks power used by the receiver.

As the default, PMOD and FOD share the same LOSS\_THR setting resistor for which the recommended starting point is 400 mW (selected by a 56.2-k $\Omega$  resistor on the LOSS\_THR option pin 43). That value has been empirically determined using standard WPC disc, ring and foil FOD test objects. Some tuning might be required in the final system as every system will be different. This tuning is best done by trial and error, use the set resistor values given in the table to increase or decrease the loss threshold and retry the system with the standard test objects. The ultimate goal of the FOD feature is safety, to protect misplaced metal objects from becoming hot. Reducing the loss threshold and making the system too sensitive will lead to false trips and a bad user experience. Find the balance which best suits the application.

If the application requires disabling one or the other or setting separate PMOD and FOD thresholds, a setting resistor of appropriate value can be connected directly from the LOSS\_THR (pin43) to the FOD (pin16) or PMOD (pin17) pins, as needed. These pins are then read at power up and the correct respective values are set. To selectively disable PMOD, for example, only the chosen FOD resistor value would be connected between LOSS\_THR (pin43) and FOD (pin 16) and PMOD (pin17) would left open.

Resistors of 1% tolerance must be used for proper detection of the desired bin.

**Table 2. Option Select Bins**

BIN NUMBER	RESISTANCE (k $\Omega$ )	LOSS THRESHOLD (mW)
0	<36.5	250
1	42.2	300
2	48.7	350
3	56.2	400
4	64.9	450
5	75.0	500
6	86.6	550
7	100	600
8	115	650
9	133	700
10	154	750
11	178	800
12	205	850
13	>237	Feature Disabled

## Shut Down via External Thermal Sensor or Trigger

Typical applications of the bq500211A will not require additional thermal protection. This shutdown feature is provided for enhanced applications and is not only limited to thermal shutdown. The key parameter is the 1.0 V threshold on pin 2. Voltage below 1.0 V on pin 2 causes the device to shutdown.

The application of thermal monitoring via a Negative Temperature Coefficient (NTC) sensor, for example, is straightforward. The NTC forms the lower leg of a temperature dependant voltage divider. The NTC leads are connected to the bq500211A device, pin 2 and GND. The threshold on pin 2 is set to 1.0 V, below which the system shuts down and a fault is indicated (depending on LED mode chosen).

To implement this feature follow these steps:

- 1) Consult the NTC datasheet and find the resistance vs temperature curve.
- 2) Determine the actual temperature where the NTC will be placed by using a thermal probe.
- 3) Read the NTC resistance at that temperature in the NTC datasheet, that is  $R_{NTC}$ .
- 4) Use the following formula to determine the upper leg resistor ( $R_{Setpoint}$ ):

$$R_{Setpoint} = 2.3 \times R_{NTC} \quad (1)$$

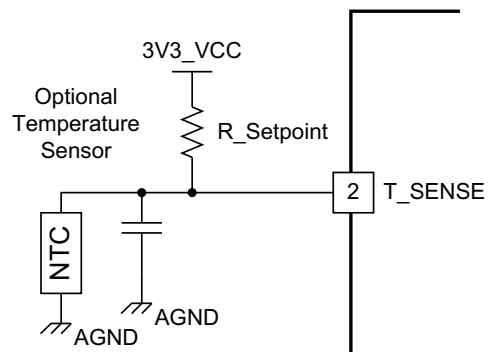
The system will restore normal operation after approximately five minutes or if the receiver is removed. If the feature is not used, this pin must be pulled high.

---

### NOTE

Pin 2 must always be terminated, else erratic behavior may result.

---



**Figure 6. Negative Temperature Coefficient (NTC) Application**

## Fault Handling and Indication

The following is a table of End Power Transfer (EPT) packet responses, fault conditions, the duration how long the condition lasts until a retry is attempted. The LED mode selected determines how the LED indicates the condition or fault.

CONDITION	DURATION (before retry)	HANDLING
EPT-00	Immediate	Unknown
EPT-01	5 seconds	Charge complete
EPT-02	Infinite	Internal fault
EPT-03	5 minutes	Over temperature
EPT-04	Immediate	Over voltage
EPT-05	Immediate	Over current
EPT-06	Infinite	Battery failure
EPT-07	Not applicable	Reconfiguration
EPT-08	Immediate	No response
OVP (over voltage)	Immediate	
OC (over current)	1 minute	
NTC (external sensor)	5 minutes	
PMOD/FOD warning	12 seconds	10 seconds LED only, 2 seconds LED + buzzer
PMOD/FOD	5 minutes	

### Power Transfer Start Signal

The bq500211A features two signal outputs to indicate that power transfer has begun. Pin 23 outputs a 400-ms duration, 4-kHz square wave for driving low cost AC type ceramic buzzers. Pin 24 outputs logic high, also for 400 ms, which is suitable for DC type buzzers with built-in tone generators, or as a trigger for any type of customized indication scheme. If not used, these pins can be left open.

### Power-On Reset

The bq500211A has an integrated Power-On Reset (POR) circuit which monitors the supply voltage and handles the correct device startup sequence. Additional supply voltage supervisor or reset circuits are not needed.

### External Reset, $\overline{\text{RESET}}$ Pin

The bq500211A can be forced into a reset state by an external circuit connected to the  $\overline{\text{RESET}}$  pin. A logic low voltage on this pin holds the device in reset. For normal operation, this pin is pulled up to 3.3 V<sub>CC</sub> with a 10-kΩ pull-up resistor.

### Trickle Charge and CS100

The WPC specification provides an End-of-Power Transfer message (EPT-01) to indicate charge complete. Upon receipt of the charge complete message, the bq500211A will change the LED indication to solid green LED output and halt power transfer for 5 seconds.

In some battery charging applications there is a benefit to continue the charging process in trickle-charge mode to top off the battery. There are several information packets in the WPC specification related to the levels of battery charge (Charge Status). The bq500211A uses these commands to enable top-off charging. The bq500211A changes the LED indication to reflect charge complete when a Charge Status message is 100% received, but unlike the response to an EPT, it will not halt power transfer while the LED is solid green. The mobile device can use a CS100 packet to enable trickle charge mode.

If the reported charge status drops below 90% normal, charging indication will be resumed.

## Current Monitoring Requirements

The bq500211A is WPC1.1 ready. In order to enable the PMOD or FOD features, current monitoring must be provided in the design.

Current monitoring is optional however, it is used for the foreign metal protection features and over current protection. The system designer can choose not to include the current monitor and remain WPC1.0 compliant. Alternately, the additional current monitoring circuitry can be added to the hardware design but not loaded. This would enable a forward migration path to future WPC1.1 compatibility.

For proper scaling of the current monitor signal, the current sense resistor should be 20 m $\Omega$  and the current shunt amplifier should have a gain of 50, such as the INA199A1. The current sense resistor has a temperature stability of  $\pm 200$  PPM. Proper current sensing techniques in the application hardware should also be observed.

## Over-Current Protection

The bq500211A has an integrated current protection feature which monitors the input current reported by the current sense resistor and amplifier. If the input current exceeds a safety threshold, a fault is indicated and power transfer is halted for one minute.

If this feature is desired, the sense resistor and amplifier are required. If this feature is not desired, the I\_SENSE input pin to the bq500410A (pin 42) should be grounded.

---

### NOTE

Always terminate the I\_SENSE pin (pin 42), either with the output of a current monitor circuit or by connecting to ground.

---

## MSP430G2001 Low Power Supervisor

This is an optional low-power feature. By adding the MSP430G2001, the entire bq500211A is periodically shut down to conserve power, yet all relevant states are recalled and all running LED status indicators remain on.

### MSP430 Low Power Supervisor Details

Since the bq500211A needs an external low-power mode to significantly reduce power consumption, one way of positively achieving that goal is to remove its supply and completely shut it down. In doing so, however, the bq500211A goes through a reset and any data in memory would be lost. Important information regarding charge state, fault condition and operating mode would be cleared. The MSP430G2001 maintains the LED indication and stores previous charge state during the bq500211A reset period.

The LEDs indicators are now driven by the MSP430G2001, do not exceed the pin output current drive limit.

Using the suggested circuitry, a standby power reduction from 300 mW to less than 90 mW can be expected making it possible to achieve Energy Star rating.

The user does not need to program the MSP430G2001, an off-the-shelf part and any of the available packages can be used as long as the connections are correct. The required MSP430G2001 firmware is embedded in the bq500211A and is boot loaded at first power up, similar to a field update. The MSP430G2001 code cannot be modified by the user.

---

### NOTE

The user cannot program the MSP430G2001 in this system.

---

## All Unused Pins

All unused pins can be left open unless otherwise indicated. Pins 1, 3, 45 can be tied to GND and flooded with copper to improve ground shielding. Please refer to the pin definition table for further explanations.



## APPLICATION INFORMATION

### Overview

The application schematic for the transmitter with reduced standby power is shown in [Figure 7](#).

#### CAUTION

Please check the bq500211A product page for the most up-to-date application schematic and list of materials package before starting a new design.

### Input Regulator

The bq500211A requires 3.3 VDC to operate. A buck regulator or a linear regulator can be used to step down from the 5-V system input. Either choice is fully WPC compatible, the decision lies in the user's requirements with respect to cost or efficiency.

For highest efficiency use a low-cost buck regulator, TPS62237, which on account of a 3-MHz switching frequency, can use a 0805 size chip inductor. This results in a very attractive combination, high performance, small size, ease of use and low cost.

### Power Train

The bq500211A drives a phase-shifted full bridge. This is essentially twin half bridges and the choice of driver devices is quite simple, a pair of TPS28225 synchronous MOSFET drivers are used with four CSD17308Q2 NexFETs. Other combinations work and system performance with regards to efficiency and EMI emissions vary. Any alternate MOSFETs chosen must be fully saturated at 5-V gate drive and be sure to pay attention whether or not to use gate resistors; some tuning might be required.

### Low Power Supervisor

Power reduction is achieved by periodically disabling the bq500211A while LED and housekeeping control functions are continued by U4 – the low-cost, low quiescent current microcontroller MSP430G2001. When U4 is present in the circuit (which is set by a pull-up resistor on bq500211A pin 25), the bq500211A at first power-up boots the MSP430G2001 with the necessary firmware and the two chips operate in tandem. During standby operation, the bq500211A periodically issues a SLEEP command, Q12 pulls the RESET pin low, therefore reducing its power consumption. Meanwhile, the MSP430G2001 maintains the LED indication and stores previous charge state during this bq500211A reset period. This bq500211A reset period is set by the RC time constant network of R26, C22 (see [Figure 7](#)). WPC compliance mandates receive detection within 500 ms, the power transmitter controller, bq500211A, awakes every 400 ms to produce an analog ping and check if a valid device is present. Increasing this time constant, therefore is not advised; shortening could result in faster detection time with some decrease in efficiency.

### Disabling Low Power Supervisor Mode

For lowest cost or if the low-power supervisor is not needed, please refer to [Figure 8](#) for the application schematic.

#### NOTE

Current sense shunt and amplifier circuitry are optional. The circuitry is needed to enable Foreign Object Detection (FOD) and a forward migration path to WPC1.1 compliance.

## PCB Layout

A good PCB layout is critical to proper system operation and due care should be taken. There are many references on proper PCB layout techniques.

Generally speaking, the system layout will require a 4-layer PCB layout, although a 2-layer PCB layout can be achieved. A proven and recommended approach to the layer stack-up has been:

- Layer 1, component placement and as much ground plane as possible.
- Layer 2, clean ground.
- Layer 3, finish routing.
- Layer 4, clean ground.

Thus, the circuitry is virtually sandwiched between grounds. This minimizes EMI noise emissions and also provides a noise free voltage reference plane for device operation.

Keep as much copper as possible. Make sure the bq500211A GND pins and the power pad have a continuous flood connection to the ground plane. The power pad should also be stitched to the ground plane, which also acts as a heat sink for the bq500211A. A good GND reference is necessary for proper bq500211A operation, such as analog-digital conversion, clock stability and best overall EMI performance.

Separate the analog ground plane from the power ground plane and use only one tie point to connect grounds. Having several tie points defeats the purpose of separating the grounds.

The COMM return signal from the resonant tank should be routed as a differential pair. This is intended to reduce stray noise induction. The frequencies of concern warrant low-noise analog signaling techniques, such as differential routing and shielding, but the COMM signal lines do not need to be impedance matched.

Typically a single chip controller solution with integrated power FET and synchronous rectifier will be used. To create a tight loop, pull in the buck inductor and power loop as close as possible. Likewise, the power-train, full-bridge components should be pulled together as tight as possible. See the bq500211AEVM-045, bqTESLA Wireless Power TX EVM User's Guide ([Texas Instruments Literature Number SLVU536](#)) for layout examples.

## References

*Building a Wireless Power Transmitter*, SLUA635

*Technology*, Wireless Power Consortium. <http://www.wirelesspowerconsortium.com/>

*An Introduction to the Wireless Power Consortium Standard and TI's Compliant Solutions*, Johns, Bill.

[BQ500210 Datasheet](#)

[BQ51013 Datasheet](#)

Typical Application Diagram

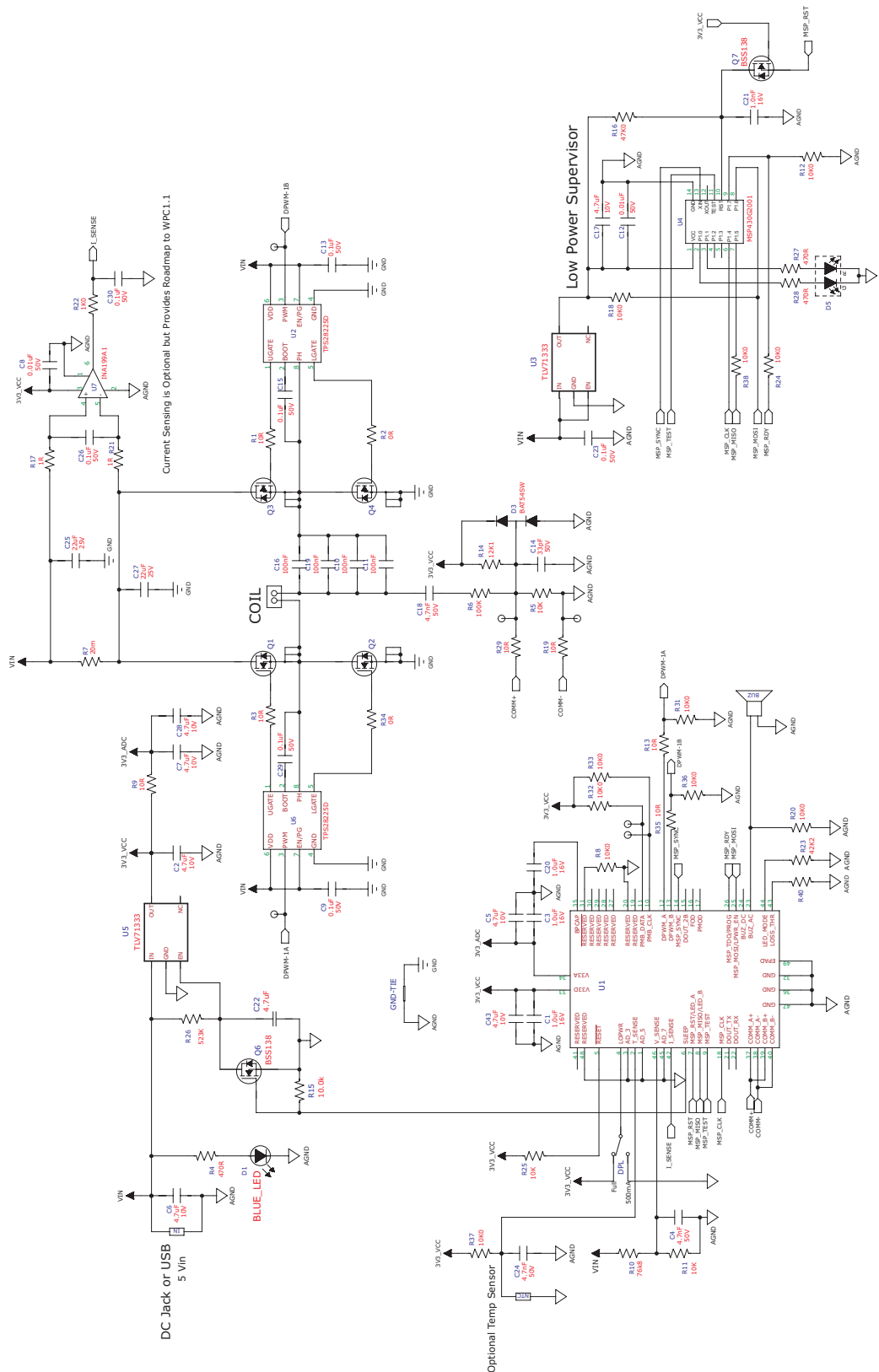


Figure 7. bq500211A Typical Low-Standby Power Application Diagram

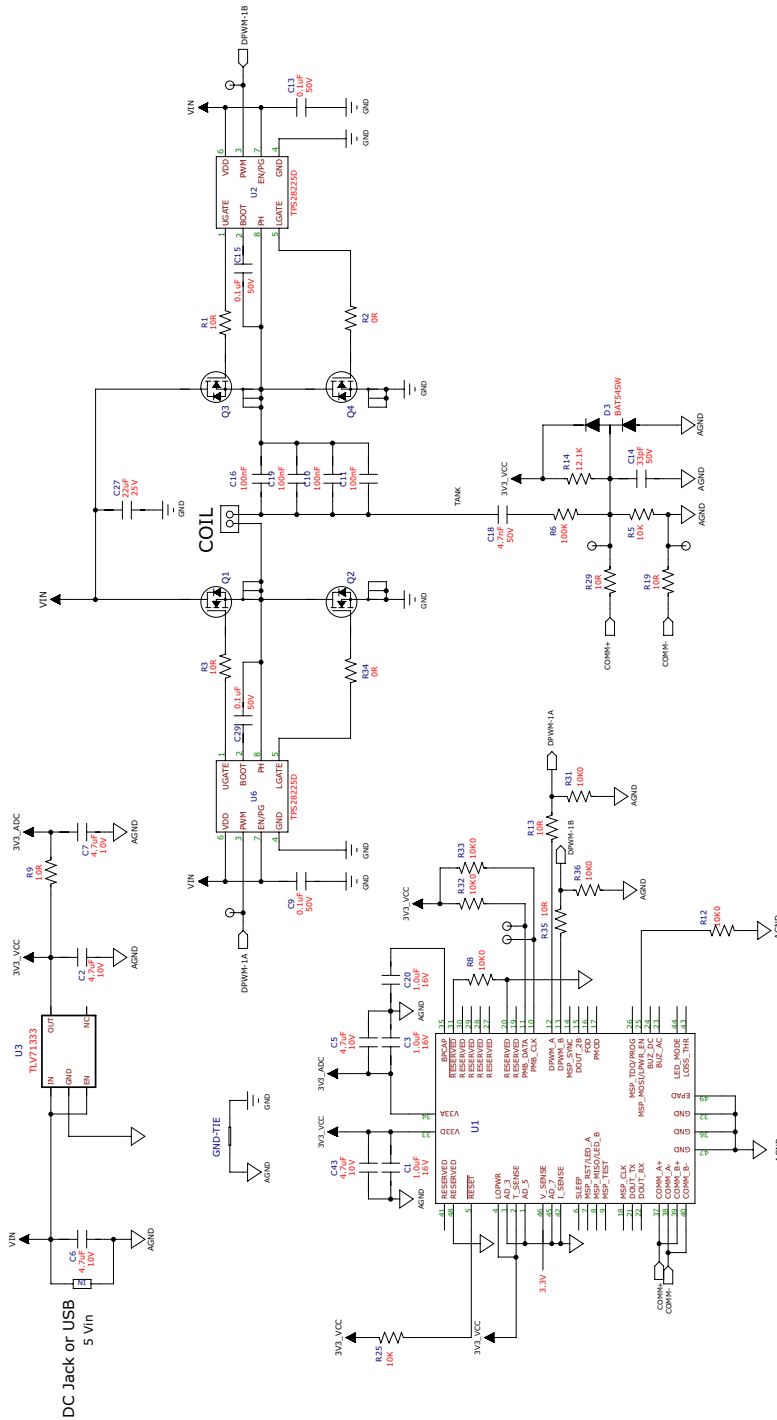


Figure 8. bq500211A Typical Low-Cost Application Diagram

### REVISION HISTORY

Changes from Original (December, 2012) to Revision A	Page
• Changed pinout diagram, pin names FOD and PMOD pin SWAP. ....	6
• Changed bq500211A Typical Low-Cost Application Diagram, V <sub>SENSE</sub> is pulled to GND. ....	20

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ500211ARGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 110	BQ500211A	<a href="#">Samples</a>
BQ500211ARGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 110	BQ500211A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ500211ARGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
BQ500211ARGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

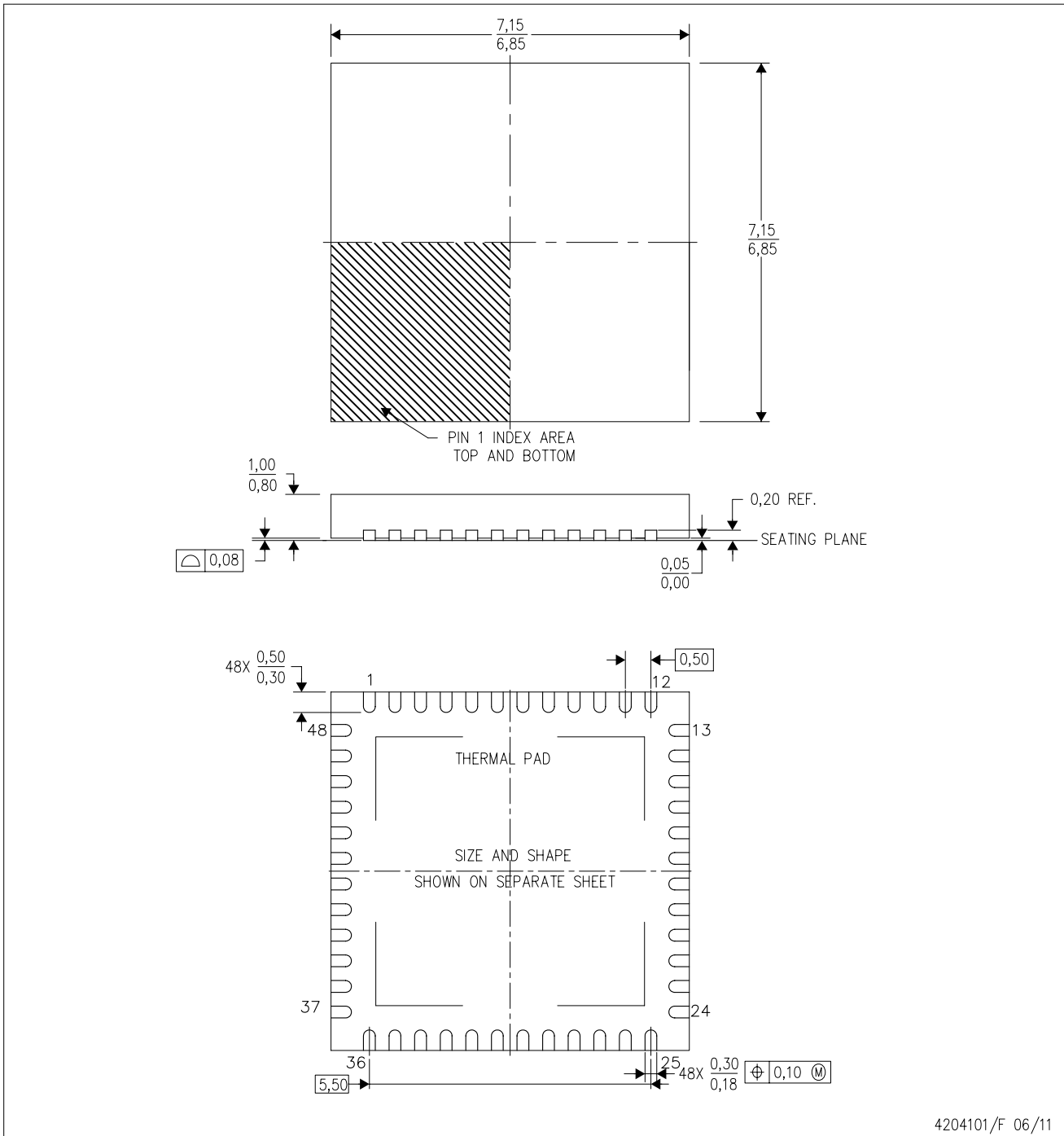
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ500211ARGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
BQ500211ARGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

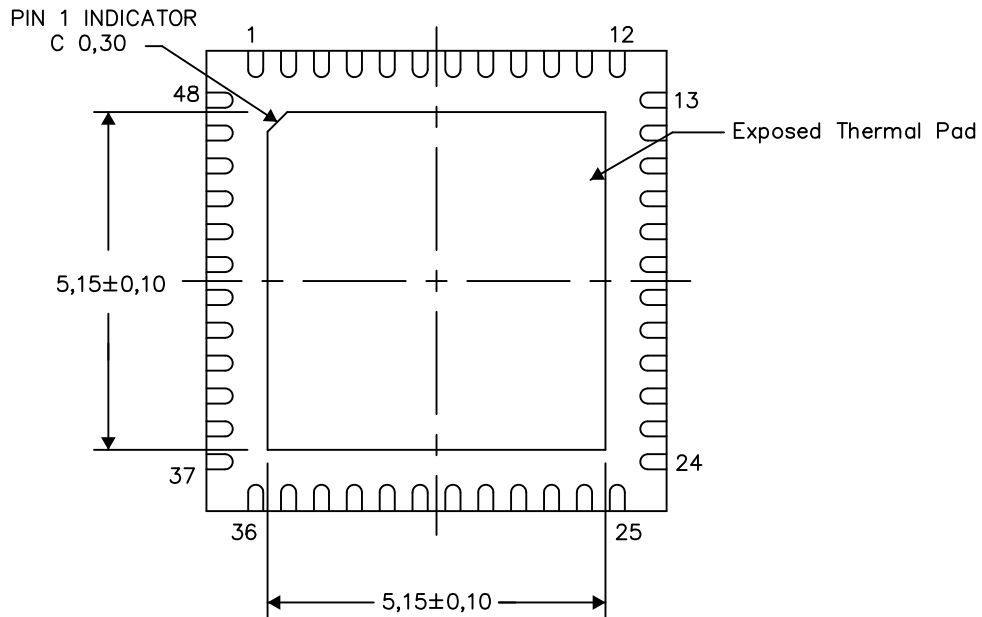


**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

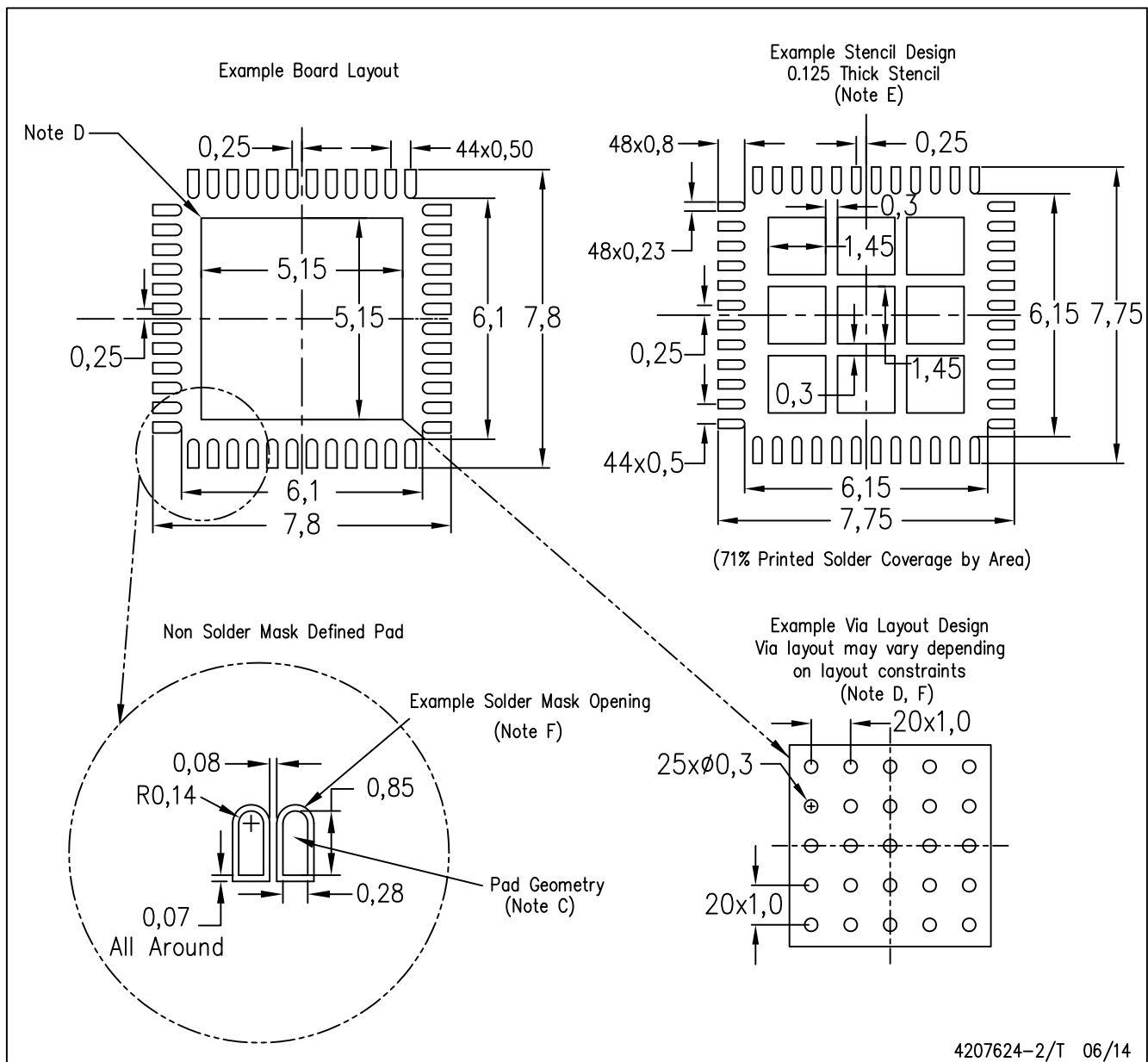
Exposed Thermal Pad Dimensions

4206354-2/Y 06/14

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4207624-2/T 06/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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